REMARKS

Claims 17-22 are pending and stand rejected under Section 102 in view of the Uchiyama reference (USP 6,748,507).

Initially, Applicant's attorney notes that a call was placed to Examiner Chankong to inquire as to the status of this application. Applicant's attorney understands that an advisory action is in process, which indicates that the after final amendment has not been entered. Accordingly, Applicant is herewith submitting a new amendment, along with an RCE. This amendment includes claim clarifications and arguments in addition to those presented in the after final amendment.

Applicant respectfully submits that the rejection under Section 102 based on Uchiyama is incorrect. Applicant's claimed invention is directed at a data processor that operates in a plurality of operation modes, and the operation mode in which the data processor operates is based on the mode register. Thus, the invention defined in Applicant's claims expressly recites a specific relationship between the mode register and operation modes of the data processor having particular characteristics. See, e.g., Fig. 4 of the specification and related description in the specification, and in particular standby control register STBYR. In accordance with the present invention, the operation mode of the data processor is based on contents of the mode register. The expressly recited operation modes that are indicated by the mode register include a first operation mode (CPU executes instructions), a second operation mode (CPU and clock pulse generator halt operation), and a third operation mode (CPU halts executing instructions and clock pulse generator generates clock signals).

Further, Applicant has clarified that the operation modes comprise operation modes of the data processor, and not operation modes of an externally connected memory.

Thus, as express language in Applicant's claims make clear, there is a specific relationship between the mode register and the operation modes of the data processor, and three distinct operation modes follow from the mode register and its settings.

The mode register of Uchiyama, on the other hand, does not provide the relationship between the mode register and the operation modes of the data processor as claimed by Applicant. The mode register of Uchiyama instead determines the operation of a synchronous DRAM that is external to the data processor (the clarifying amendment proposed herein by

Applicant, "formed on a single chip," serves to further emphasize this point of distinction over Uchiyama). The mode register of Uchiyama does not indicate the operation modes of the data processor. The mode register of Uchiyama is for a different purpose and does not fulfill the relationship with the operation modes recited in the presently pending claims.

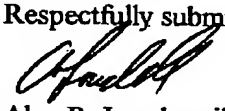
Accordingly, Applicant submits that the rejection in view of Uchiyama should be withdrawn. Uchiyama's mode register relates to controlling the operation of the external synchronous DRAM, and Uchiyama does not disclose or suggest Applicant's invention. Accordingly, Applicant submits that its invention, as defined in the presently pending claims, patentably distinguishes over Uchiyama and the other cited references.

If there are any questions or issues regarding the foregoing, Applicant requests an opportunity to discuss such matters with the Examiner by way of an in-person or telephone interview.

Please charge any additional fees due, or credit any overpayment, to Deposit Account No. 50-0251.

No new matter has been added.

Respectfully submitted,



Alan R. Loudermilk
Registration No. 32,788
Attorney for Applicant(s)

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P.O. Box 3607
Los Altos, CA 94024-0607
408-868-1516